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Optimum Zigzag Scan Mapping Method on FPGA Device

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***Abstract* — Growing telecommunications facilities currently used to transmit multimedia data. One example is the multimedia data transmission of image data, generally an image containing a large amount of data that requires a line of communication and storage media with large memory size. Therefore, efforts to reduce the size of image data (compressing image data) is needed. One of the stages in image compressing is zigzag scan image which serves to classify the components of the quantized coefficients ranging from low frequency to the high frequency. This article proposes the optimization zigzag scan using mapping method. The purpose of optimalization zigzag scan is for implementation into an FPGA and than can speed up the time of JPEG image compression process, finally a JPEG file size smaller is obtained. Mapping is made by placing the input data in accordance with the order of the zigzag position. The overall mapping process is implemented into the FPGA. Based on the simulation results, the input data can be placed in the order position has been determined for the same number of clock cycles with the number of input data (for 8*8 image size is 64 clock cycles).**

Keywords—FPGA, image, mapping, telecomunication, zigzag

I. INTRODUCTION

Telecommunications facilities developed at this time is not only used to send messages in voice or text, but also used to transmit multimedia data. One example is the multimedia data transmission of image data, generally an image contains a large amount of data, in terms of the number of pixels as well as from the large number of bits used. This resulted in increasingly large amounts of data that require communication channels and storage media with large memory size. Thus the necessary effort to reduce the size of image data is needed. Compressing is one way to reduce the size of image data to improve the efficiency of delivery and storage of image data without reducing the quality of the image itself.

Image compression is the application of data compression performed on digital images with the aim of reducing redundancy of the image data, in this study used image data is a JPEG image. Image compression was developed to address the problems above and also can be useful to accelerate the delivery of image data in multimedia communications and does not require a large storage medium for storing the image data. One of the stages in image compression is the process of cleaning the DCT coefficients that are not essential for the formation of a new image; a high frequency will be selected to be eliminated [7].

To facilitate the removal of the high frequency of the process undertaken is to adopt the model zigzag scan to classify the components of the coefficients quantized ranging from low frequency to the high frequency Zigzag scan is a process that changes the matrix of 8 x 8 results quantization process into the vector 1 x 64, with reading zigzag scanning. In the zigzag scan process is coefficient quantized DCT zeroes tend to be read in sequence. The problem now is how to compress the image data by optimizing the zigzag scan.

Image compression can be done both software and hardware. Graphic designers commonly used compression software to manipulate and store the image files on the computer. Hardware JPEG compression method can also be done in two ways. First, the compression algorithm implemented on a microcontroller or DSP through the program [8]. The second way is the JPEG algorithm implementation on a digital circuit (ASIC or FPGA) that is widely used in various devices [1]. Compression operation can be performed quickly and real-time wearing a digital circuit such as ASIC or FPGA. When a FPGA is configured, the internal circuitry is connected in a way that creates a hardware implementation of the software application[4]. Implementation of the digital circuit has been chosen for a better performance in terms of time compression [3]. Results zigzag optimization coding will be implemented into the FPGA. Implementation into FPGA is designed as efficiently as possible so as to optimize the use of resources on the FPGA.

The general objective of this research is to develop a technique for optimizing zigzag scan at one stage of the JPEG image compression. This technic will be implemented into the FPGA. This implementation can accelerate JPEG image compression time in order to obtain results with a JPEG file sizes smaller. The required storage medium from the JPEG data is not big and the image data can be quickly transmitted through communications media.

II. METHODOLOGY

A. Zigzag Reordering

Zigzag scan is the process that converts 8 x 8 matrix results into the vector quantization process 1 x 64, with readings in a zig-zag scanning. Zigzag scan is a grouping of components of the quantized coefficients ranging from low frequency (DC) up to high frequency (AC). Figure 1 shows the process of reading in a zigzag, the index coefficient sorting runs starting from the top left and moving in the direction of the arrows in the picture, until then end up on the bottom right corner of the data matrix. While the standard sequence of coefficients that came out after the zigzag scan shown in Figure 2.

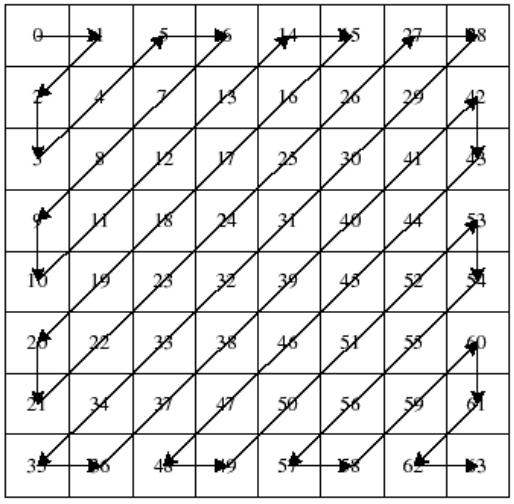

Fig. 1. Zigzag scan process on a 8x8 image

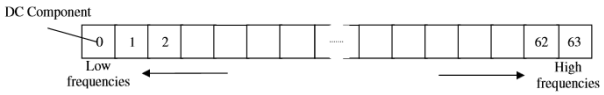

Fig. 2. The order of the coefficients after zigzag scan

B. JPEG

The term "JPEG" means Joint Photographic Experts Group. JPEG mainly used for lossy compression of digital photography (image). The degree of compression can be adjusted, allowing a selectable tradeoff between storage size and image quality. JPEG typically achieves 10:1 compression with little perceptible loss in image quality. JPEG compression is used in a number of image file formats. JPEG is the most common image format used by digital cameras and other photographic image capture devices; along with JPEG, it is the most common format for storing and transmitting photographic images on the Web. These format variations are often not distinguished, and are simply called JPEG.

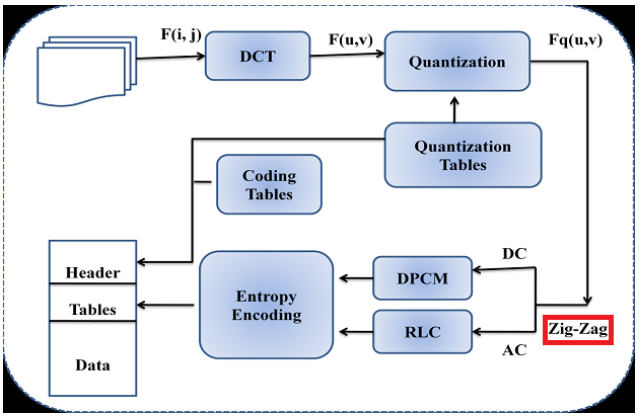

Fig. 3. Architecture JPEG compression with zigzag section to be optimized [2]

III. DISCUSSION AND RESULT

In the study conducted by the Ketul Shah and Sagar Shah MATLAB programming for the zigzag scan, the overall process of zigzag scan is performed, the adjustment conditions and looping done while the results are displayed in the form of an array only on the conditions in accordance with the variable d which is the sum of the line the columns being processed. The more adjustments as conditions and loops that do will result in resources being used more and more if the zigzag scan process is applied to hardware such as FPGA[4].

To overcome this in order to use resources on the hardware is not much, the method used is through a mapping method. With this mapping method matrix data to be displayed directly placed at a predetermined zigzag. Mapping method is done to define in advance the order in which the data matrix is processed and will be displayed in the form of an array. The sequence data are defined according to the zigzag scan process sequence. This mapping method will reduce the process of adjusting the process conditions and reduce recurrence. The fewer processes that take place then the use of resources on the hardware become less. Here's programming to sort the data matrix into an array using the mapping method:

```
clc;clear all;
im = [1 2 3 4 5 6 7 8; 9 10 11 12 13 14 15 16; 17 18 19 20
21 22 23 24; 25 26 27 28 29 30 31 32; 33 34 35 36 37 38
39 40; 41 42 43 44 45 46 47 48; 49 50 51 52 53 54 55 56;
57 58 59 60 61 62 63 64];
pos = [1 2 6 7 15 16 28 29; 3 5 8 14 17 27 30 43; 4 9 13 18
26 31 42 44; 10 12 19 25 32 41 45 54; 11 20 24 33 40 46
53 55; 21 23 34 39 47 52 56 61; 22 35 38 48 51 57 60 62;
36 37 49 50 58 59 63 64];
t=0;
for i=1:length(im_vhdl)
    for j=1:length(im_vhdl)
        t=t+1;
        mapping_mat (t) = im_vhdl(i,j);
    end
end
mapping_mat
```

The results of the program change 8 x 8 matrix into vector 1 x 64 (array) using a mapping method as shown in Figure 4. Programmers using MATLAB will process the input matrix so that it will produce output in the form of an array in accordance with the order of zigzag scan.

The placement process matrix data into the array can be done quickly because the data matrix was placed directly on the existing position and in accordance with the order of zigzag scan. Because the array results are in accordance with the order of zigzag scan, the results of the array can be used to classify the components of the quantized coefficients ranging from low frequency to the high frequency.

Implementation zigzag scan using mapping method to the FPGA through VHDL programming. Data input is a matrix (2D) with a size of 8x8. This matrix was changed to an array (1D) so that size to 1x64. Changes in the form of a matrix input data into the array is intended to adjust the characteristics of the input data and meet with the requirement at the FPGA. In FPGA normally uses the concept of the serial data and based on clock signal. Data coming into the FPGA is individually alternately and sequentially.

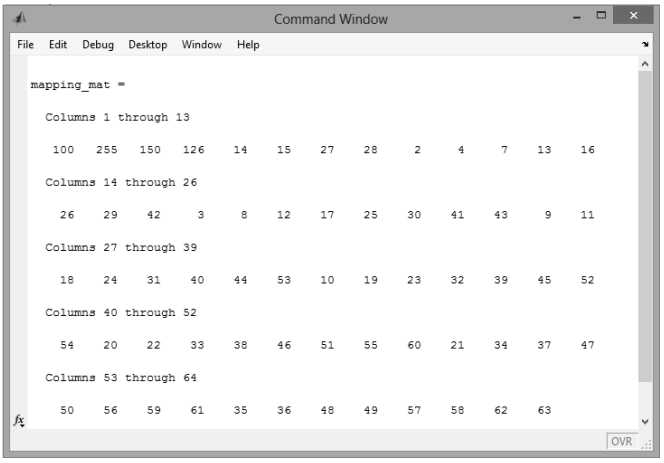

Fig. 4. Results zigzag scan using the mapping method

Once the input data is defined and then proceed to define the sequence of positions. This position is used to put the input data in accordance with the order of the position that has been determined. The result of this input data placement into outputs to zigzag scans using the mapping method. At the design stage using VHDL, sequence position data is placed on addressing the block position. Where later input data contained in input blocks will be matched with a sequence of position data in block position to get the output of the zigzag scan with the mapping method in order to get the results of grouping the components of the coefficients quantized ranging from low frequency (DC) to the frequency high (AC).

VHDL programming for component design of zigzag scan using mapping method as follows:

```
if (i<8) then
  if (j<8) then
        reg(rom_posisi(i,j)) <= im(i,j);
        j<=j+1;
  else
        j<=0;
        i<=i+1;
       end if;
  else
  i<=0;
  end if;
end if;
```

Using VHDL programming, the first step is to read the input data and move based on the position of rows and columns sequentially. The reading sequence is bassed on the counter, that will read 64 times in accordance with the format of the input data and sequence position in 8x8 matrix. For 8x8 matrix there will be 64 input data and sequence position to be read. After reading all the input data and the position of the input data, All the data are sequenitaly mapped based on positions and the results are stored in a register.

The next step is to show the results of the mapping that is stored in the register with variable mapping_out as in the following code :

```
if (ii<64) then
   mapping_out <= conv_std_logic_vector(reg(ii),8);
   ii<=ii+1;
   else
   ii<=0;
end if;
```

The simulation results of the zigzag scan using mapping method shown in Figure 5 and 6. The simulation results show that the first 64 clock cycles to do the process of reading the input data and sequence first position as shown in Figure 5. After the first 64 clock cycles recently displayed mapping results. Even if the first 64 clock cycles existing mapping results are displayed, the results are not valid mapping. After passing through the first 64 clock cycles newly obtained results are valid mapping. All the input data are placed in the order position that has been defined (see Figure 6).

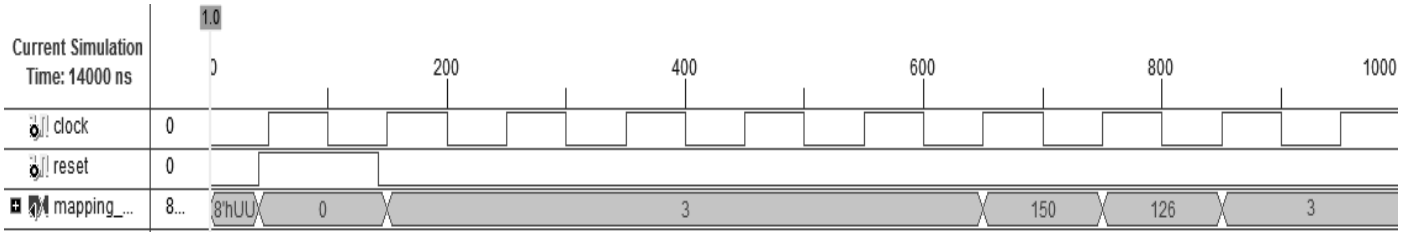

Fig. 5. The simulation results on the first 64 clock cycles

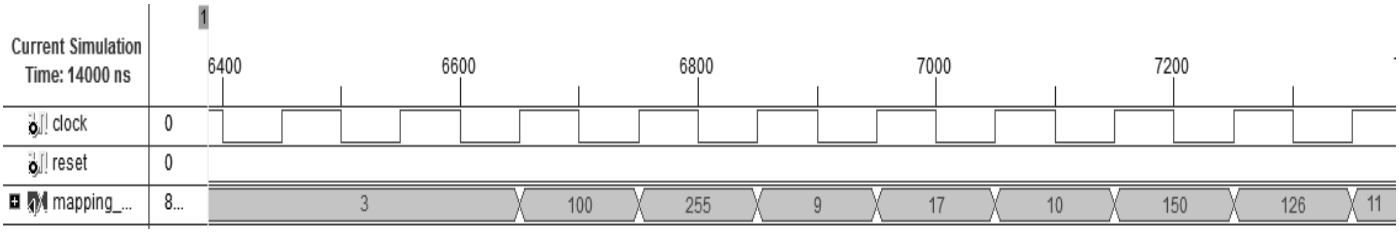

Fig. 6. The simulation results zigzag scan using the mapping method

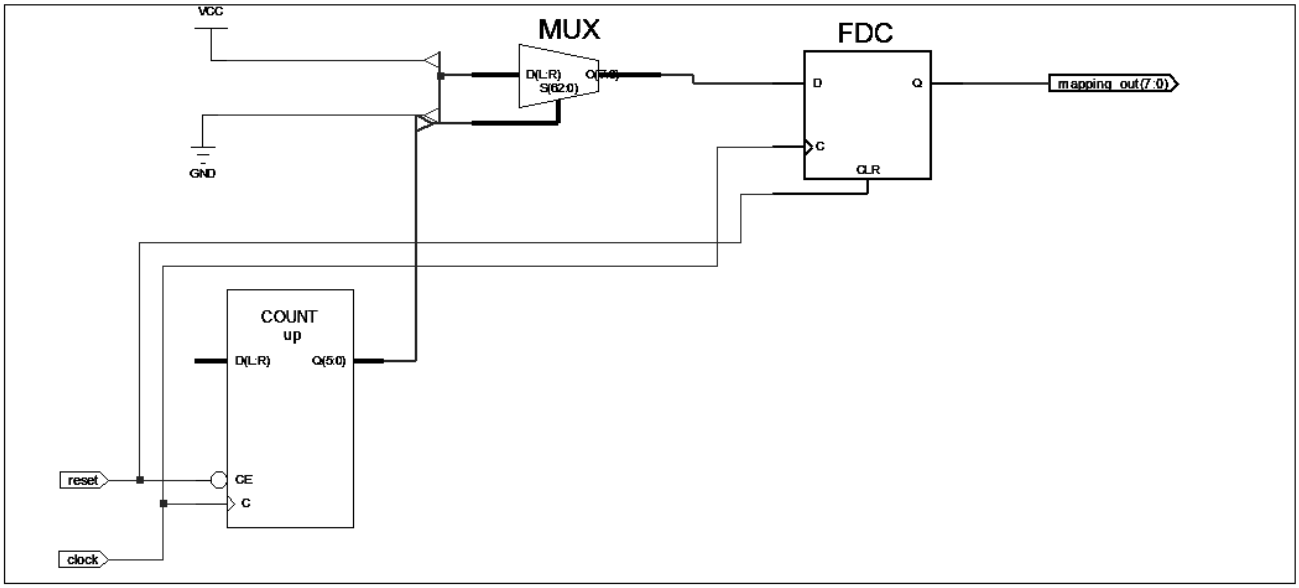

Fig. 7. Zigzag scan schematic using the mapping method

PETA Project Status			
Project File:	Peta.ise	**Current State:**	Synthesized
Module Name:	Pemetaan	**• Errors:**	No Errors
Target Device:	xc3s500e-5cp132	**• Warnings:**	2126 Warnings
Product Version:	ISE 9.2i	**• Updated:**	Wed Jun 22 13:23:12 2016

PETA Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	0	4656	0%
Number of Slice Flip Flops	1	9312	0%
Number of bonded IOBs	10	92	10%
Number of GCLKs	1	24	4%

Fig. 8. Summary of resources utilization.

The RTL (Register Transfer Logic) circuit is obtained from the synthesis results, shown in Figure 7. This circuit consists of one counter to perform the calculation of index (i & j), one multiplexer and one D flip-flop to map the 8*8 image size in pre store input data according to pre store position index.

Summary of resources used to implement the zigzag scan using mapping method as shown in Figure 8. Implementation of zigzag scan using the mapping method requires 1 Slice

Flip-flops, 10 bonded IOBs and 1 GCLKs. In other word, the resource utilization is less than 10% for xc-3s500e-5cp132 FPGA board.

IV. CONCLUSION

An IP core for Zigzag scan using mapping methode component has been obtained. The readyness of mapping result is according to the number of data input, for 8*8 image size is 64 clock cycles. This design only use one Slice Flip-Flops, 10 bonded of IOBs and 1 GCLKs.

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